Notice of Allowability	Application No.	Applicant(s)	
	10/771,662	DAW, BRADLEY M.	
	Examiner	Art Unit	
	Jefferey F. Harold	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *application filed February 4, 2004*.

2. ☒ The allowed claim(s) is/are *1-30*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Information Disclosure Statement

1. The references listed in the Information Disclosure Statement submitted on February 4, 2004 have been considered by the examiner (see attached PTO-1449).

Allowable Subject Matter

2. ***Claims 1-30*** are allowed.

3. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the prior art discloses a voltage monitoring system configured for monitoring a DC voltage of a differential line pair with respect to a threshold voltage, comprising: a detection circuit comprising a first line and a second line, each line connectable to one of the two lines of the differential line pair, the detection circuit further comprising: a low pass filter configured and disposed in relation to the first and second lines to pass a DC signal of steady state or low-frequency voltage swing from the differential line pair to the rest of the detection circuit, and to block a pulse signal from a microcontroller from passing between the first and second lines, however, the prior art of record failed to disclose or fairly suggest a bias circuit portion comprising at least one Zener diode, disposed between the first and second lines and configured to allow current to flow, and accordingly to pass the pulse signal, between the first and second lines when the voltage across the differential line pair is above a selected breakdown voltage of the Zener diode; a DC isolation portion comprising a pair of capacitors disposed in the first and second lines, the DC isolation portion configured to pass the pulse signal, and to impede other DC signals from the differential line pair from

passing from the differential line pair to the microcontroller; and, the microcontroller, configured to send and detect pulse signals, and to detect when the DC voltage across the line pair is at least one of above and below the threshold value, and to thus enable monitoring of the differential line pair in this respect; the low pass filter being disposed between the line pair and the other elements of the detection system, the bias circuit portion being disposed between the low pass filter and the DC isolation portion, and the DC isolation portion being disposed between the bias circuit portion and the microcontroller, pulse signals being passed or not passed between the first and second lines depending on whether the DC voltage across the differential line pair is above or below the breakdown voltage of the bias circuit diode being detectable by the microcontroller, and the low pass filter impeding the pulse signals from traveling out onto the differential line pair and the DC isolation portion impeding DC signals from interfering with the microcontroller and isolating the differential line pair from the microcontroller and other elements which are connectable thereto.

Regarding claim 10, the prior art of record discloses a telephone system monitoring system configured to detect at least one of on hook and off hook DC states of a differential POTS line pair, comprising: a detection circuit configured to isolate the line pair from the rest of the detection circuit by means of capacitors in the line pair; however, the prior art of record failed to disclose or fairly suggest wherein the detection circuit further comprising means for sending pulse signals across the capacitors and means for returning or preventing return of the pulse signals depending upon whether the DC voltage differential across the line pair is above or below a selected threshold

value; means for indicating whether the voltage across the differential line pair is at least one of above or below the threshold value.

Regarding claim 28, the prior art of record discloses a system configured for a detection of at least one of a ring condition and off hook condition on a differential line pair in a telephone network comprising: a low pass filter comprising a first and second resistor on a first line of a differential line pair and a third and fourth resistor on a second line of the differential line pair, wherein a first capacitor is electrically coupled to the first line and second line between the first and second resistor of the first line and the third and fourth resistor of the second line; however, the prior art of record failed to discloses or fairly suggest a bias circuit portion electrically coupled to an output of the low pass filter comprising a first Zener diode in series with and in opposite polarity from and a second Zener diode, each Zener diode having a break down voltage so that a change in voltage can be detected on either the first line and the second line of the differential line Pair; a DC isolation circuit portion electrically coupled to an output of the bias circuit comprising a second capacitor on the first line of the differential line pair and a third capacitor on the second line of the differential line pair; a protection circuit portion connected to an output of the DC isolation circuit for protecting surges and spikes in a differential line; and a microcontroller for detecting the state of the differential line pair having a digital output coupled to the second line for generating pulses and having an input electrically coupled to the first line of the differential line pair for detecting whether the pulses are present at a voltage level greater than a preset level.

Regarding claim 29, the prior art of record discloses a system configured for a detection of at least one of a ring condition and off hook condition on a differential line pair in a telephone network, comprising: a low pass tilter electrically coupled to a bias circuit; however, the prior art of record failed to disclose or fairly suggest the bias circuit wherein a first Zener diode is in series with and in opposite polarity from and a second Zener diode, each Zener diode having a break down voltage so that a change in voltage can be detected between on either a first line and a second line on a differential line pair; a DC isolation circuit electrically coupled to the bias circuit and electrically coupled to a protection circuit for protecting surges and spikes in the differential line; and a microcontroller having a digital output coupled to a line on the differential line pair for generating pulses and having an input electrically coupled to the other line of the differential line pair for detecting whether the pulses are present at a voltage level greater than a preset level.

Regarding claim 30, the prior art of record discloses a method for measuring a change in DC voltage on a differential line pair used in a telephone network connected to a microcontroller, comprising the steps of: injecting a pulse signal from a microprocessor onto a first line of a differential line pair; however, the prior art of recording fails to disclose or fairly suggest biasing the differential line pair with a bias circuit comprising a first Zener diode that is in series with and in opposite polarity to a second Zener diode, each Zener diode having a break down voltage so that a change in voltage can be detected on either the first line or a second line of the differential line pair; isolating the microcontroller from a DC voltage on the differential line pair;

protecting the microcontroller from surges and spikes on the differential line pair; detecting the microcontroller-generated pulse on the second line of the differential line pair with the microprocessor when the voltage difference between the first line of the differential line pair and the second line of the differential line pair is greater than a preset level.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jefferey F. Harold whose telephone number is 571-272-7519. The examiner can normally be reached on Monday - Friday 9 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh H. Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jefferey F Harold
Primary Examiner
Art Unit 2646

JFH
March 17, 2006